**Lab report no 4**



**Fall 2022**

**CSE-308L Digital Systems Design Lab**

**Submitted By**

**Names Registration No**

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Section: **A**

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**Lab Task:**

1- Using switches enter a BCD number and show the resulting

number on the seven segment display.

2- Connect the output of your lab 02 (4 bit adder) to the seven

segment display. Note that number above 1001 are not valid

BCD numbers. In this situation keep the seven segment display

off and just the dp on.

**Task no 1: -**

module DECODER7\_out(out,in,dp,en);

output [6:0] out;

output dp;

input [3:0] in;

input en;

assign dp=en;

assign out =

(in==0)?(7'b1000000):

(in==1)?(7'b1111001):

(in==2)?(7'b0100100):

(in==3)?(7'b0110000):

(in==4)?(7'b0011001):

(in==5)?(7'b0010010):

(in==6)?(7'b0000010):

(in==7)?(7'b1111000):(7'b1111111);

endmodule

**Task no 2: -**

module FullAdderr(Sum, Cout, X, Y, Cin);

output Sum, Cout;

input X, Y, Cin;

//Behavoural Code

assign {Cout,Sum}=X+Y+Cin;

endmodule

module RippleCAdder (Cout, S, X, Y);

output Cout;

output [3:0] S;

input [3:0] X, Y;

wire [2:0] C; //Intermediate/Internal Carries

// FA1 (Sum, Cout, X, Y, Cin); //FA1's Interface (I/O Pins)

FullAdderr fulla0 (S[0], C[0], X[0], Y[0], 1'b0);

FullAdderr fulla1 (S[1], C[1], X[1], Y[1], C[0]);

FullAdderr fulla2 (S[2], C[2], X[2], Y[2], C[1]);

FullAdderr fulla3 (S[3], Cout, X[3], Y[3], C[2]);

endmodule

module DECODER7\_out(out,dp,en,Cout,X,Y);

output Cout;

wire [3:0] S;

input [3:0] X, Y;

RippleCAdder rc(Cout,S,X,Y);

output [6:0] out;

output dp;

input en;

assign dp=en;

assign out =

(S==0)?(7'b1000000):

(S==1)?(7'b1111001):

(S==2)?(7'b0100100):

(S==3)?(7'b0110000):

(S==4)?(7'b0011001):

(S==5)?(7'b0010010):

(S==6)?(7'b0000010):

(S==7)?(7'b1111000):

(S==8)?(7'b0000000):

(S==9)?(7'b0011000):(7'b1111111);

endmodule